ABSTRACT

A signal pathway is presented for routing clock signals from a clock driving means to a circuit component and on to a termination. The signal pathway employs a minimal stub to carry the clock signals to the circuit component without introducing excess signal distortions. A first signal line of the signal pathway is formed on a circuit board and extends from the clock driving means to a first terminal for interfacing with the circuit component. A second signal line of the signal pathway is routed on the circuit component from one end adjacent to and electrically coupled with the first terminal to an opposite end adjacent to and electrically coupled with a second terminal formed on the circuit board. The stub extends from the second signal line on the circuit component. A third signal line of the signal pathway extends on the circuit board from the second terminal to the termination.